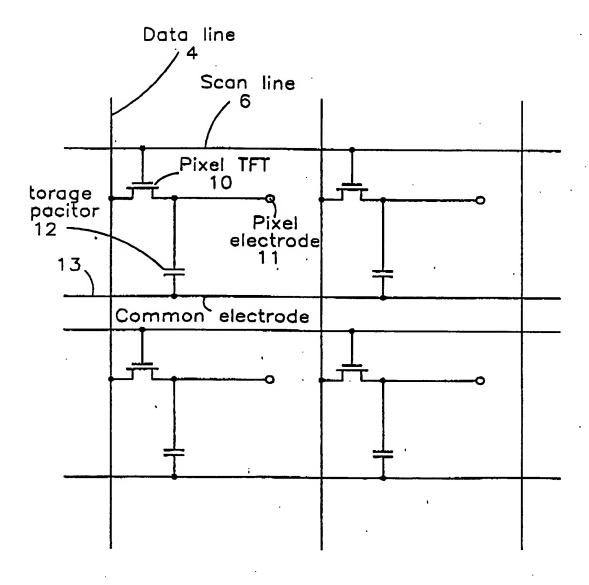


FIG 1



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FIG 2



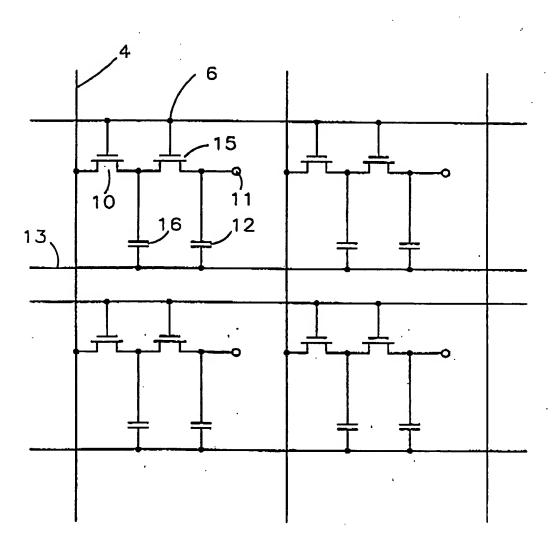
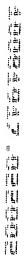
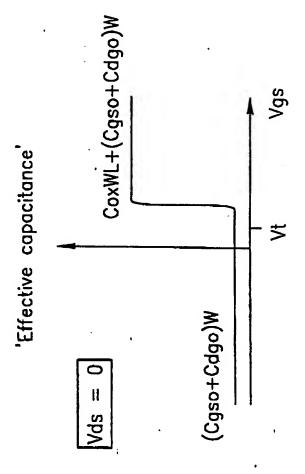
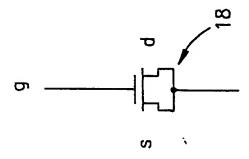


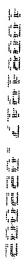
FIG 3











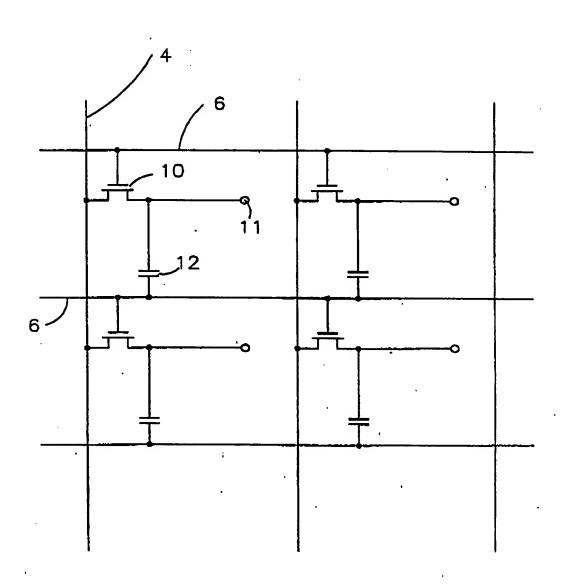


FIG 5

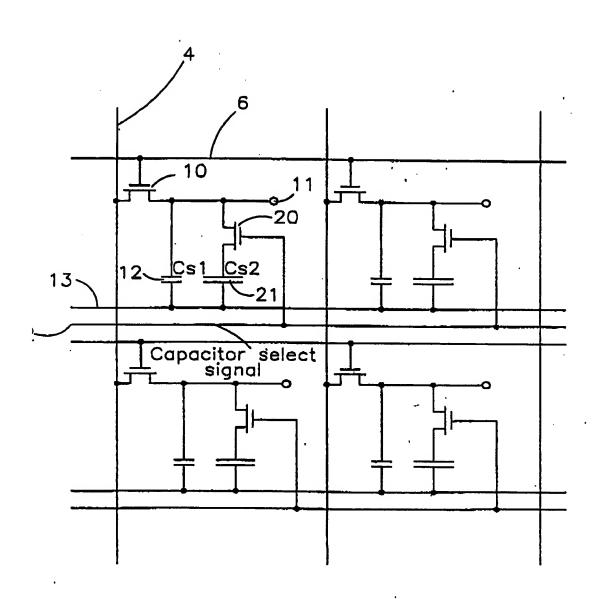
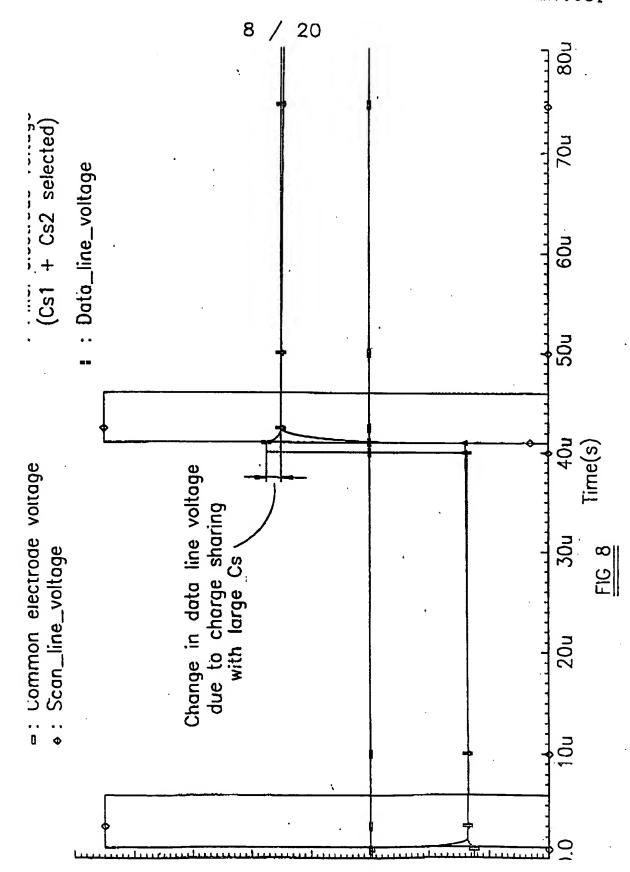


FIG 6



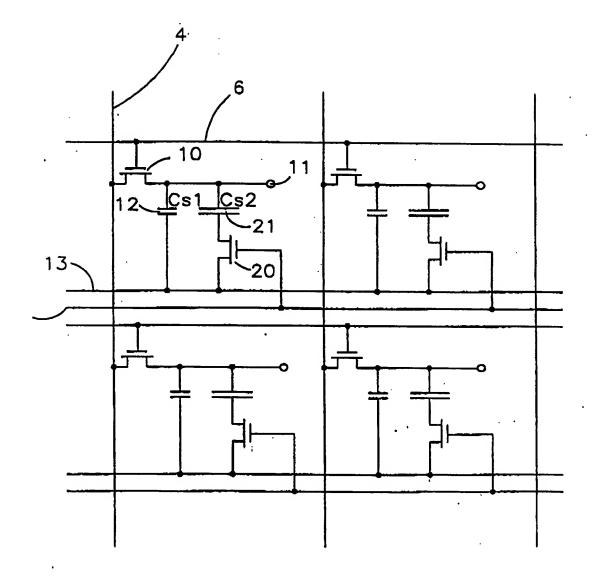
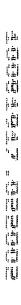


FIG 9

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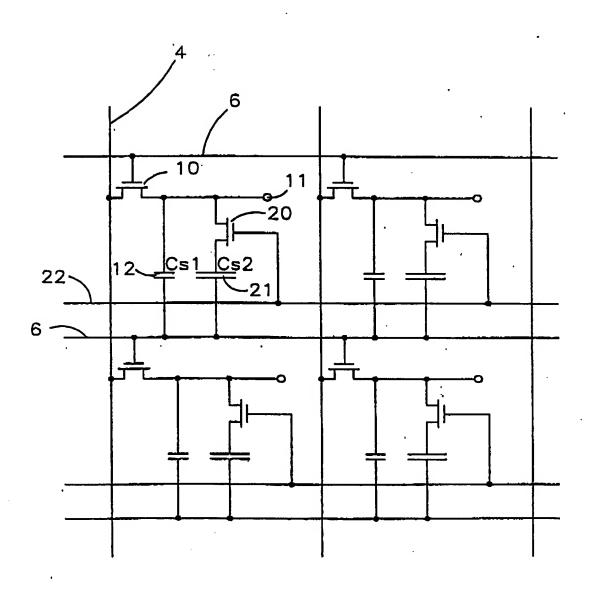
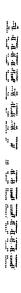
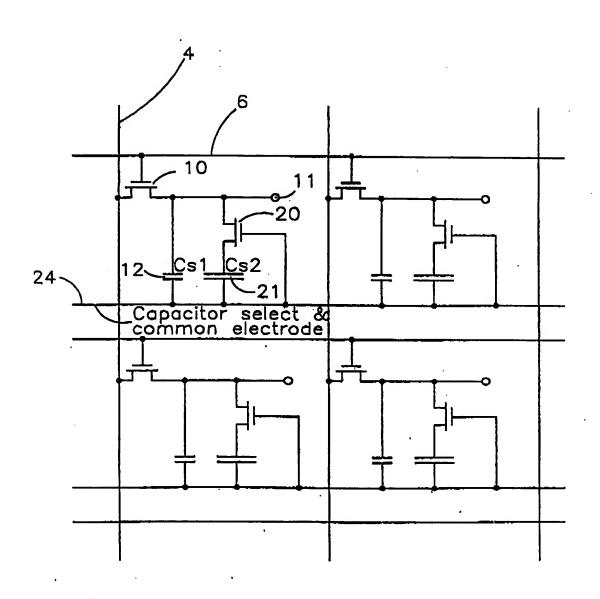


FIG 10





. FIG 11

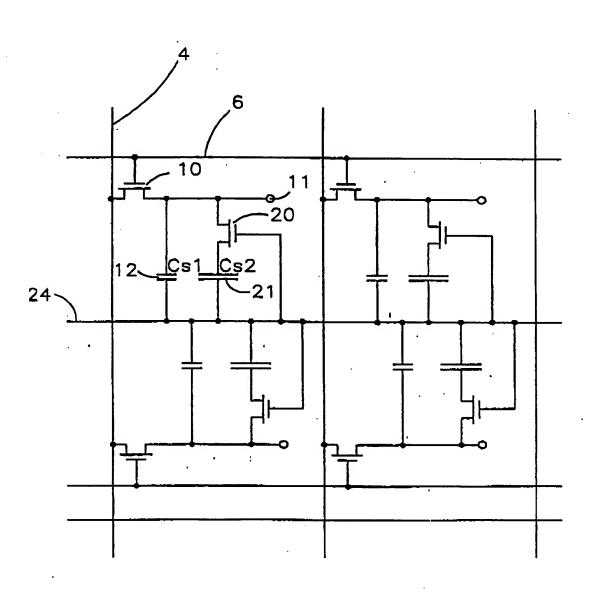


FIG 12

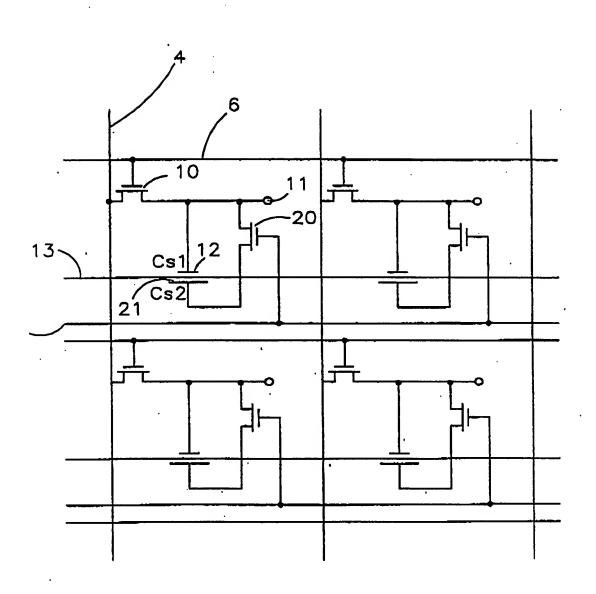


FIG 13

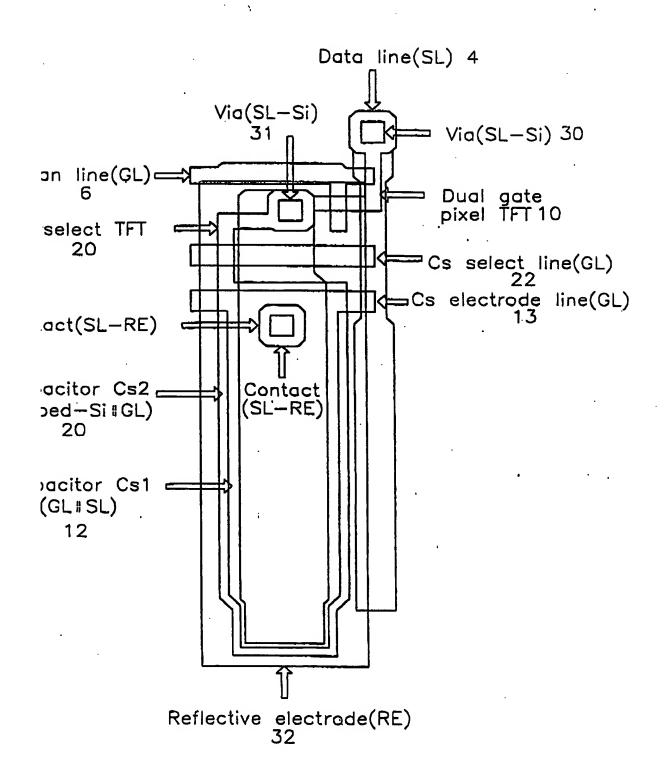


FIG 14

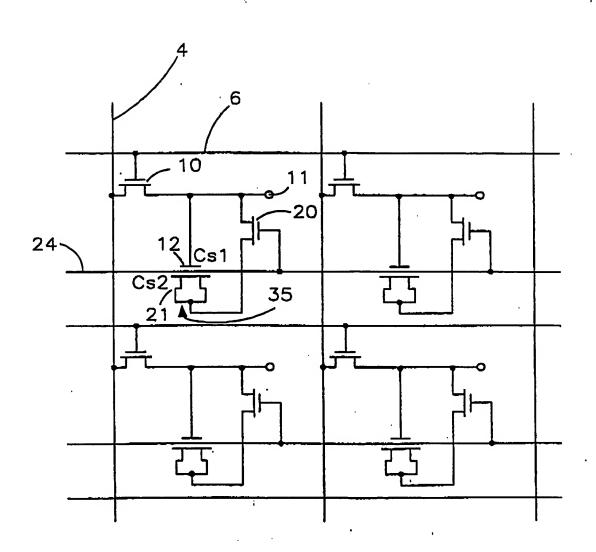
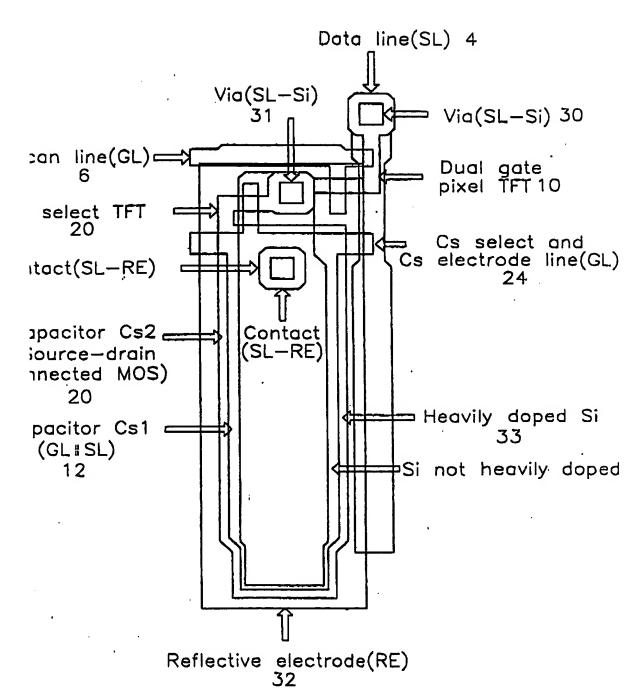
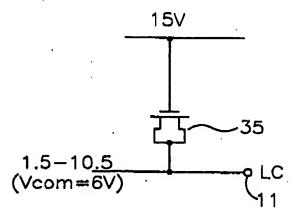


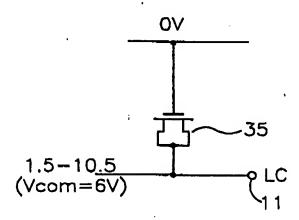
FIG 15



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Condition for high capacitance: Vt<4.5



Condition for low capacitance: Vt>-1.5

FIG 17

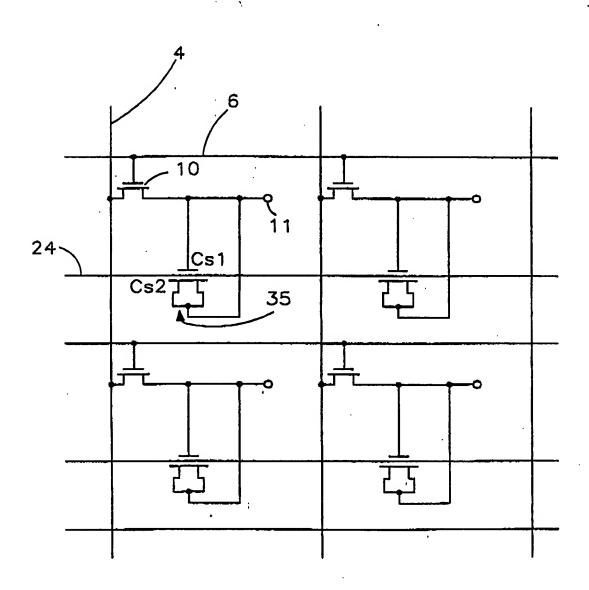


FIG 18

19 / 20

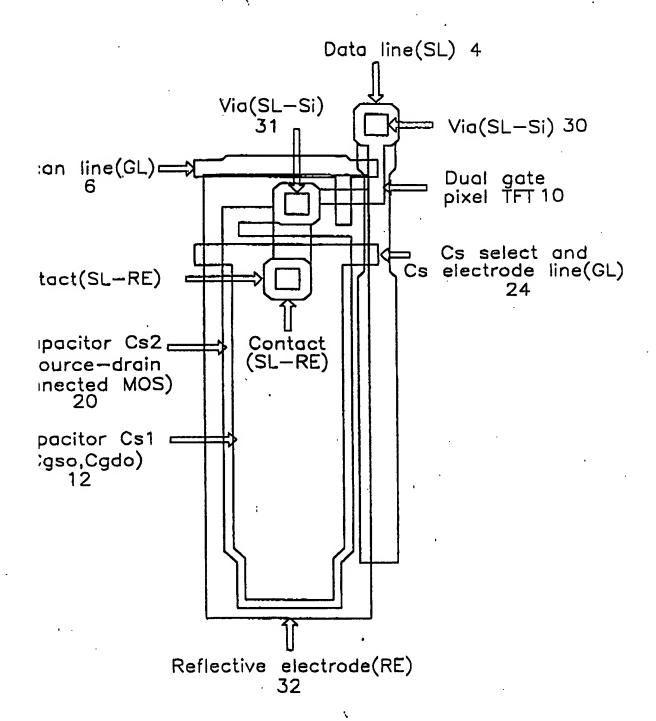
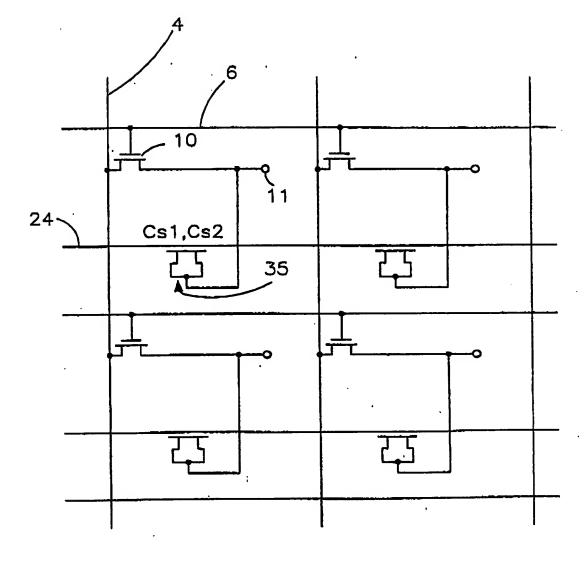


FIG 10



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FIG 20